PATENT APPLICATION
Attny Docket No. SLA0468

#11/Appeal Brief
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: PATENT APPLICATION

Inventors: Apostolos Voutsas, Yukihiko Nakata, and Takeshi Hosoda

Serial No: 09/696,813 Group No.: 2823

Filed: October 25, 2000 Examiner: K. Nguyen

Title: A SEMICONDUCTOR DEVICE AND A METHOD OF CREATING THE SAME UTILIZING METAL INDUCED CRYSTALLIZATION WHILE SUPPRESSING PARTIAL SOLID PHASE CRYSTALLIZATION

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

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David C. Ripma, Reg. No. 27,672
Signature Date January 20, 2003

APPEAL BRIEF
(37 C.F.R. §1.192)

Commissioner for Patents
Washington, DC 20231

ATTENTION: Board of Patent Appeals and Interferences

Applicants respectfully submit this appeal brief in support of the appeal to the final rejection of the claims in the above identified application. The Notice of Appeal was filed in this case on January 15, 2003.

REAL PARTY IN INTEREST

Upon the filing of the patent application, as referenced above, all interest in the present invention had been assigned by the above-named inventors to Sharp Laboratories of America, Inc., of Camas, WA., a subsidiary of Sharp Electronics Corporation of Mahwah, NJ, which is a subsidiary of Sharp Corporation of Osaka, Japan.

RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the above-mentioned patent application.

STATUS OF CLAIMS

The patent application was filed with claims 1-19.

After a restriction requirement, which requested election of either claims 1-8 and 12 directed to method claims, or claims 9-11 and 13-19 directed to devices, Applicants elected to pursue claims 1-8 and 12 directed to a method of fabricating a polysilicon film.

Claims 9-11 and 13-19 have been cancelled.

Claims 20-22 were added in the Response dated July 24, 2002.

Claims 1-8, 12 and 20-22 are pending.

No claims have been allowed.

Claims 1-8, 12 and 20-22 stand rejected.

Claims 1-8, 12 and 20-22 are currently on appeal.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to final rejection.

SUMMARY OF INVENTION

An embodiment of the present invention is a method of fabricating a polysilicon film as illustrated in FIG. 7. In particular, a metal induced crystallization (MIC) process is provided which employs an amorphous silicon (a-Si) film precursor deposited by physical vapor

deposition (PVD), wherein the precursor film does not readily undergo crystallization by standard solid phase crystallization (SPC) processes. After formation of the silicon film by PVD, a metal catalyst is introduced to the PVD deposited a-Si precursor. The a-Si film is then subject to annealing which transforms the amorphous silicon to poly silicon (p-Si) by the MIC method wherein the crystalline growth occurs fastest at regions that have been augmented with a metal catalyst and proceeds extremely slowly, practically zero, at regions which bear no metal catalyst. In one embodiment the metal catalyst may be introduced to selected regions of the a-Si through a window in a barrier layer. By use of the PVD a-Si precursor in the process of the present invention, the MIC process may take place at higher annealing temperatures and shorter annealing times without SPC taking place. The process has a faster throughput than previous MIC processes, results in a p-Si film having virtually no catalyst impurities remaining in the film, and a film having spatially uniform characteristics.

ISSUES

Issue 1 – Whether claims 1-8, 12 and 21 are patentable under 35 U.S.C. §103(a) over Zhang et al., in view of Applicant's admitted prior art (AAPA) and Venkatesan?

Issue 2 – Whether claim 20 is patentable under 35 U.S.C. §103(a) over Zhang et al.?

Issue 3 – Whether claim 22 is patentable under 35 U.S.C. §103(a) over Zhang et al.?

GROUPING OF CLAIMS

Claims 2-8, 12 and 21 depend from base claim 1. Claims 20 and 22 are both independent claims.

However, all claims stand independently, as will be explained in the Arguments section of this Brief, and do not stand or fall together.

ARGUMENTS

REJECTIONS UNDER 35 U.S.C. §103

Issue 1: The method of claim 1 is nonobvious over Zhang et al. in view of Applicant's admitted prior art and Venkatesan et al.

The Examiner bears the initial burden of establishing a *prima facie* conclusion of obviousness. (See MPEP §2142). To establish a *prima facie* case of obviousness, three basic criteria must be met. There must be some teaching or suggestion to modify the reference or combine reference teachings. There must be a reasonable expectation of success. The prior art reference must teach or suggest all claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claim 1 was rejected under 35 U.S.C §103(a) as being unpatentable over Zhang et al. (U.S. Patent No. 5,569,610) in view of Applicant's admitted prior art and Venkatesan et al. (U.S. Patent No. 5,371,382).

Applicants realize that one cannot show nonobviousness by attacking references individually where rejections are based upon combinations or references. *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co., Inc.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986) However, to improve the ease of explanation, Applicants will address each cited reference in turn, so that the weakness of each reference may be made clear, and the lack of teaching or suggestion to combine may be shown.

Applicants' claim 1 recites a multi-step process: "depositing an amorphous silicon film on the substrate by the process of physical vapor deposition" and then the separate step of "introducing a metal catalyst to the amorphous silicon film." In other words, the amorphous

silicon film <u>is already fully formed</u> when the metal catalyst is introduced. This two step process is not taught or suggested in the prior art.

In the first step, the use of physical vapor deposition (PVD) is claimed to form the amorphous silicon layer. As recited by Applicants in numerous locations throughout the patent application, the use of PVD to form the amorphous silicon film gives unexpected and beneficial results over amorphous silicon films formed by chemical vapor deposition (CVD). In particular, Applicants refer to page 18, line 10, through page 19, line 5, of Applicants' specification:

> "The process of producing the PVD-Si precursor film and the film's physical properties will now be described. The [amorphous silicon] a-Si precursor of the present invention is an a-Si film deposited using physical vapor deposition (PVD). In other words, PVD technology is utilized for the formation of the thin silicon film that is used as the active layer of the TFT device. This type of silicon material is very difficult to crystallize by [solid phase crystallization] SPC alone, due to the way in which the film is deposited. When silicon is sputtered, two phenomena occur which relate to the physical properties of the film. First, silicon atoms arrive on the surface of the forming films having a higher energy than in relevant, chemical deposition methods. This energy is imparted to the film creating collision cascades and resulting in structural damage to the film. This structural damage is similar to the damage experienced by a film subjected to ion implantation. However, the amount of damage to the film during PVD is lower than during ion implantation due to the lower energy of the arriving silicon species during PVD. Second, energetic neutral atoms of the plasma forming gas reflected from the target reach the film and also impart their energy and contribute to the structural changes in the film. As a result of these two phenomena, the structural disorder in the film increases, making it particularly difficult to form stable nuclei and commence solid phase crystalline [SPC] growth when the film is subjected to a thermal anneal. <u>**Surprisingly, however, the structural disorder in the film does not prohibit crystallization by the method of metal induced crystallization [MIC]**</u>." (emphasis added).

In a second step, the metal catalyst is introduced to the previously formed PVD deposited "amorphous silicon film." Applicants' two step process, wherein the amorphous silicon film is

initially formed without having catalytic material formed therein, is important due to utilization of a barrier layer later in the process. Specifically, the catalytic material may be subsequently added to the amorphous silicon film in selected regions through such windows, as recited in Applicants' dependent claim 12. None of the references cited by the Examiner, either alone or in combination, teach or suggest, first, "depositing an amorphous silicon film on the substrate by the process of physical vapor deposition" and then, second, a separate step of "introducing a metal catalyst to the amorphous silicon film" as recited in Applicants' claim 1.

The Examiner states that the Zhang et al. reference teaches "depositing an amorphous silicon film by the process of physical vapor deposition such as sputtering on the substrate" <u>and then</u> "introducing a metal catalyst . . . into the amorphous silicon film." The Examiner mischaracterizes the prior art.

Physical vapor deposition (PVD) is mentioned only one time in the entire Zhang et al. specification. At col. 2, line 65 through col. 3 line 2, Zhang et al. states: "When the amorphous silicon film is formed by CVD the catalytic material is added to the raw material gases. When the amorphous silicon film is formed by physical vapor deposition such as sputtering, the catalytic material may be added to the target or evaportation source for forming a film." Accordingly, Zhang et al. teach a one step process of forming the catalytic material within the silicon film because both the silicon material and the metal catalyst are present on the target or evaporation source. Zhang et al. does not mention or suggest any benefits of a two step process wherein the a-Si film is first formed by PVD and then a metal catalyst is introduced to the previously formed silicon film. Zhang et al. do not recite any benefits at all for forming the a-Si film from PVD. In fact, Zhang et al. appears to teach away from a two step process because the one step PVD process of Zhang et al. recited above can be conducted more quickly. Each of

Zhang's four examples recite forming an amorphous silicon film by low pressure chemical vapor deposition (LPCVD), a very different process than Applicants' process utilizing physical vapor deposition (PVD).

To summarize the Zhang et al. reference, the Examiner has not cited any teaching in Zhang et al. that would tend to teach one of ordinary skill in the art that a two step process comprising forming an a-Si film by PVD and then adding a metal catalyst, is preferred in the process of forming a poly silicon film. Zhang et al. appears to indicate that forming the a-Si film by either PVD or CVD is insignificant, that CVD is preferred, and that if PVD is used, the metal catalyst should be formed simultaneously with the a-Si film. Applicants argue, as they did in their response to the first office action, that Zhang et al. teaches away from the desirability of a two step process, in that Zhang et al. teach the benefits of a one step process, i.e., the ease of forming the a-Si film containing a metal catalyst, in one single step. Nothing has been cited in Zhang et al. that teaches, or suggests, the significance of introducing a metal catalyst to a previously deposited film wherein the film has been deposited using physical vapor deposition (PVD).

In the Examiner's rejection, the Examiner states: "AAPA [Applicants' admitted prior art] teaches a method of fabricating a poly-silicon film in which the metal catalyst is introduced into an amorphous silicon film through a barrier layer having windows." Applicants' Background section does not mention physical vapor deposition (PVD) but instead only discusses chemical vapor deposition (CVD). Applicants' Background section, therefore, cannot teach or suggest depositing an a-Si film by physical vapor deposition and then, in a second step, introducing a metal catalyst thereto. Moreover, combining the AAPA discussion of introducing a metal catalyst to a CVD deposited a-Si film with the teaching of Zhang et al., which only discusses

examples of CVD deposited a-Si films, only suggests adding a metal catalyst to a silicon film formed by CVD. The mere fact that the prior art may be modified in the manner suggested by the Examiner, i.e., a two step process wherein the silicon is deposited by PVD and then a metal catalyst is introduced, does not make the modification obvious unless the prior art suggests the desirability of the modification. *In re Fritch*, 972 F.2d 1260, 23 USPQ2d 1780 at 1783-84 (Fed. Cir. 1992). The only suggestion of the benefits of any such combination is to be found in the detailed description portion of Applicants' disclosure.

The Venkatesan et al. reference is not concerned with metal induced crystallization, as recited in Applicants' claim 1, and in fact Venkatesan et al. does not even mention a metal catalyst. Instead, Venkatesan is directed toward doping using Boron and Arsenic to create a rectifying contact. Venkatesan is not concerned with exploiting different crystallization speeds between a catalyzed region and a non-catalyzed region. One skilled in the art would not look to Venkatesan et al.'s method of creating a rectifying contact using "dopants" which remain in the film, in order to improve a method of reducing crystallization by solid phase crystallization using a metal "catalyst" that preferably is completely depleted. Moreover, Venkatesan teaches a one step process wherein the Boron and Arsenic dopants are deposited in a single step with the silicon to form the doped silicon film. ("Sputter deposited B-doped and As-doped amorphous silicon contacts about 2000 Angstroms thick were formed on the natural IIb diamond samples. . . . The targets used for depositing the B-doped silicon and the As-doped silicon were highly B-doped silicon (100) and highly As-doped silicon (100), respectively." col.6, lines 5-12.). Accordingly, even if Venkatesan et al. were combined with Zhang et al. and the AAPA, none of these references teach or suggest a two step process wherein a metal catalyst is introduced to a

previously deposited silicon film wherein the silicon film was deposited by physical vapor deposition.

In summary, Zhang et al. teaches forming, in a single PVD deposition step, a silicon film having a metal catalyst therein. Zhang et al. does not teach or suggest first, "depositing an amorphous silicon film on the substrate by the process of physical vapor deposition" and then, a second, separate step of "introducing a metal catalyst to the amorphous silicon film." Applicants' Background section does not even address physical vapor deposition. Venkatesan et al. teaches a single deposition step wherein Boron and Arsenic are deposited simultaneously with amorphous silicon to form a rectifying contact. Venkatesan et al. does not address metal induced crystallization or metal catalysts and does not teach or suggest a two step process of "introducing a metal catalyst to the [already formed] amorphous silicon film." None of the cited references teach or suggest the surprising benefits of a two step process wherein a metal catalyst is introduced to a silicon film previously formed by PVD. Even if the one step deposition from Venkatesan's rectifying contact process is combined with Zhang et al. and the AAPA, the combination does not result in a two step PVD process as cited by Applicants. Applicants contend that the Examiner's final conclusion has not been supported by any combination of the cited prior art, but rather by reference to Applicants' own teachings. None of the three cited references, either alone or in combination, teach or suggest Applicants' two step method as recited in claim 1 and Applicants respectfully request reversal of the Examiner and allowance of independent claim 1, and corresponding dependent claims 2-8, 12 and 21.

Several of the dependent claims will now be addressed separately.

With regard to Applicants' claims 5 and 6, none of the cited references teach or suggest, in combination with the other limitations of the claims, "using Argon as the sputtering gas."

(Claim 5 also recites that the Argon content "after the deposition step is in the range of $2x10^{18}$ at/cm^3 to $5x10^{21}$ at/cm^3" and claim 6 also recites that the Argon content "after the annealing step is in the range of $2x10^{18}$ at/cm^3 to $5x10^{20}$ at/cm^3"). As stated by the Examiner, "Zhang fails to teach that the amorphous silicon film is deposited using Argon as a sputting gas." Similarly, Applicants' Background section does not address the use of Argon as a sputtering gas.

Venkatesan et al. teaches a completely different process than that of Zhang et al. or Applicants. In particular, Venkatesan et al. teach a method of creating a rectifying contact using "dopants" which remain in the film. Moreover, Venkatesan teaches a one step process wherein the Boron and Arsenic dopants are deposited in a single step with the silicon to form the doped silicon film. ("[U]sing Argon (Ar) as the sputtering gas," "Sputter deposited B-doped and As-doped amorphous silicon contacts about 2000 Angstroms thick were formed on the natural IIb diamond samples. . . The targets used for depositing the B-doped silicon and the As-doped silicon were highly B-doped silicon (100) and highly As-doped silicon (100), respectively." col.6, lines 5-12.). Venkatesan et al. do not teach or suggest using Argon to deposit a silicon film having no dopants (or a metal catalyst) therein. Vankatesan et al. do not address a method of reducing crystallization by solid phase crystallization using a metal "catalyst" that preferably is completely depleted. One skilled in the art would not look to the method of Venkatesan et al., which is concerned with simultaneously depositing Boron and Arsenic dopants in silicon to form a rectifying contact, in order to modify Zhang et al's method of depositing metal catalysts in silicon. Moreover, even if the teachings of Venkatesan et al. and Zhang et al. were combined, the result would be a single step process wherein Argon is used as the sputtering gas to simultaneously deposit a metal catalyst and the silicon, which is different from Applicants'

claimed two step process wherein Argon is used to deposit an a-Si film having no metal catalyst therein.

None of the three cited references teach or suggest Applicants' method as recited in dependent claims 5 or 6 and for this separate reason Applicants respectfully request reversal of the Examiner and allowance of dependent claims 5 and 6.

With regard to Applicants' claim 7, none of the cited references teach or suggest, in combination with the other limitations of the claim, an annealing step conducted "at a temperature <u>greater than 650 °C</u> and for a time period greater than 200 seconds" (emphasis added) wherein crystallization takes place "by pure metal induced crystallization." Zhang et al. teaches laser irradiation as the primary crystallization method, wherein a preliminary thermal anneal may be used ("It is also possible to make a preliminary anneal at 350°-650° C., preferably 400°-550° C., for 1 to 24 hours, preferably 2 to 8 hours, before the laser irradiation." col. 4, lines 1-3). Accordingly, the anneal temperatures cited by Zhang et al. for annealing of the a-Si film fall below the temperature range of "greater than 650 °C", as claimed in Applicants' claim 7. Zhang et al. teaches away from higher annealing temperatures in stating that when higher temperatures are used "the usable substrate is limited to quartz [not amorphous silicon]" (col. 2, lines 24-23.)

Venkatesan et al. disclose a heating step carried out to "activate additional dopant atoms positioned within the amorphous silicon layer," wherein the heating step "is carried out at a temperature of about 400° C. to 550° C." (Col. 2, line 64 through col. 3, line 2). Accorrdingly, the anneal temperatures cited by Venkatesan et al. for annealing of the a-Si film fall below the temperature range of "greater than 650 °C", as claimed in Applicants' claim 7.

Applicants' Background section teaches away from an anneal temperature greater than 650 °C because an anneal conducted at "a temperature in a range of 650 to 700 °C" will result in an unusable polysilicon film that "retains a relatively large amount of the metal catalyst as an impurity and has spatial irregulariteis due to formation of the crystalline structure by both MIC [metal induced crystallization] and SPC [solid phas crystallization] processes." (page 4, lines 18-21). As shown in Applicants' numerous figures, and in particular in figure 3, only Applicants' unique process utilizing an a-Si film formed by physical vapor dpeosition [PVD] results in crystallization of the amorphous silicon film, without breakdown of the silicon film, by pure metal induced crystallization at a process temperature greater than 650 °C.

None of the three cited references teach or suggest Applicants method as claimed in dependent claim 7 and for this separate reason Applicants respectfully request reversal of the Examiner and allowance of dependent claim 7.

With regard to Applicants' claim 8, none of the cited references teach or suggest, in combination with the other limitations of the claim, an annealing step that "produces a crystallization growth front length of at least 80 μm." Zhang et al., Vankatesan et al. and Applicants' Background section do not address growth fronts of "at least 80 μm." Zhang et al. and Vankatesan et al. do not even address the importance of growth front length. The only discussion of the importance of the growth front length is Applicants' disclosure which states that a growth front length of "at least 80 μm" is made possible by Applicants' two step process wherein the amorphous silicon is first deposited by PVD, and then the metal catalyst is introduced to the silicon in a second step. The Examiner's assertion that the claimed growth front may be achieved through "routine experimentation and optimization" completely ignores the fact that the cited prior art does not even mention growth front length as a important variable.

One skilled in the art would not put time and effort into "routine experimentation and optimization" of a varible having no apparent importance. The only teaching of the imoportance of the growth front length is in Applicants' disclosure. None of the three cited references teach or suggest a method that achieves the growth front length recited in claim 8 and for this separate reason Applicants respectfully request reversal of the Examiner and allowance of dependent claim 8.

With regard to Applicants' claim 12, none of the cited references teach or suggest, "providing a barrier layer on said [PVD deposited] amorphous silicon film wherein said barrier layer includes a window therein for the introduction of said catalyst to said [PVD deposited] amorphous silicon film." Modifying the Zhang et al. and Venkatesan et al. references by introduction of a metal catalyst to the PVD deposited a-Si films of these cited references through a window in a barrier layer is not possible because Zhang et al. and Venkatesan et al. both teach a one step process wherein the catalyst/dopant is introduced to the PVD a-Si film at the same time that the PVD a-Si film is formed. Applicant's Background section does not even mention PVD deposited a-Si films. Accordingly, none of the three cited references teach or suggest Applicants method as recited in dependent claim 12 and for this separate reason Applicants respectfully request reversal of the Examiner and allowance of dependent claim 12.

Issue 2: The method of claim 20 is nonobvious over Zhang et al.

Independent claim 20 recites the limitations of original claim 1 as filed and the additional limitation "wherein the annealing step is conducted at a temperature greater than 650 °C and for a time period greater than 200 seconds and less than 800 seconds." As discussed above with respect to claim 1, Zhang et al. does not teach or suggest a two step process wherein an a-Si film is deposited by physical vapor deposition and, thereafter, a metal catalyst is introduced to the

previously formed PVD deposited a-Si film. Moreover, as discussed above with respect to claim 7, Zhang et al. teaches laser irradiation as the primary crystallization method, wherein a preliminary thermal anneal may be used ("It is also possible to make a preliminary anneal at 350°-650° C., preferably 400°-550° C., for 1 to 24 hours, preferably 2 to 8 hours, before the laser irradiation." col. 4, lines 1-3). Accordingly, the anneal temperatures cited by Zhang et al. for annealing of the a-Si film fall below the temperature range of "greater than 650 °C", as recited by Applicants' claim 7. Zhang et al. teaches away from higher annealing temperatures in stating that when higher temperatures are used "the usable substrate is limited to quartz [not amorphous silicon]" (col. 2, lines 24-23.) For these reasons Applicants respectfully request reversal of the Examiner and allowance of claim 20.

<u>Issue 3:</u> The method of claim 22 is nonobvious over Zhang et al.

Claim 22 recites "A method of fabricating a polysilicon film, comprising the steps of: providing a substrate; depositing an amorphous silicon film on the substrate by the process of physical vapor deposition; <u>after deposition of said amorphous silicon film</u>, depositing a metal catalyst film <u>on selected regions</u> of the amorphous silicon film; and annealing the amorphous silicon film and the metal catalyst film to form a crystallized silicon film by pure metal induced crystallization in said selected regions." As discussed above with respect to claim 1, Zhang et al. do not teach or suggest a two step process wherein the metal catalyst is deposited "after deposition of said [PVD deposited] amorphous silicon film." Moreover, Zhang et al. does not teach or suggest depositing a metal catalyst film "on selected regions" of the amorphous silicon film. Moreover, modification of the Zhang et al. reference to deposit a metal catalyst on "selected regions" of a PVD amorphous silicon film would be impossible because Zhang et al. teach adding the metal catalyst to the target for simultaneous formation of the metal catalyst

within the PVD deposited a-Si film. For these reasons Applicants respectfully request reversal of the Examiner and allowance of claim 22.

CONCLUSION

For the extensive reasons advanced above, Applicants respectfully contend that the Examiner has not met the necessary burden for a *prima facie* case of obviousness, and further that each claim is nonobvious in light of the cited prior art and is otherwise patentable. Therefore, reversal of all rejections is courteously requested.

Respectfully submitted,

Date: 1/20/03

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

1. A method of fabricating a polysilicon film, comprising the steps of:

providing a substrate;

depositing an amorphous silicon film on the substrate by the process of physical vapor deposition;

introducing a metal catalyst to the amorphous silicon film; and

annealing the amorphous silicon film to form a crystallized region by pure metal induced crystallization.

2. The method of claim 1 further comprising the step of irradiating the crystallized region with an excimer laser after the step of annealing the amorphous silicon film.

3. The method of claim 1 further comprising the step of fabricating a thin film transistor in the crystallized region.

4. The method of claim 1 further comprising the step of utilizing the crystallized region in a liquid crystal display.

5. The method of claim 1 wherein the amorphous silicon film is deposited using Argon as a sputtering gas, and wherein the Argon content in the amorphous silicon film after the deposition step is in the range of $2x10^{18}$ at/cm^3 to $5x10^{21}$ at/cm^3.

6. The method of claim 1 wherein the amorphous silicon film is deposited using Argon as a sputtering gas, and wherein the Argon content in the crystallized region after the annealing step is in the range of $2x10^{18}$ at/cm^3 to $5x10^{20}$ at/cm^3.

7. The method of claim 1 wherein the annealing step is conducted at a temperature greater than 650 °C and for a time period greater than 200 seconds.

8. The method of claim 1 wherein the annealing step produces a crystallization growth front length of at least 80 μm.

12. The method of claim 1 further comprising the step of providing a barrier layer on said amorphous silicon film wherein said barrier layer includes a window therein for the introduction of said catalyst to said amorphous silicon film.

20. A method of fabricating a polysilicon film, comprising the steps of:

providing a substrate;

depositing an amorphous silicon film on the substrate by the process of physical vapor deposition;

depositing a metal catalyst film on the amorphous silicon film; and

annealing the amorphous silicon film and the metal catalyst film to form a crystallized silicon film by pure metal induced crystallization, wherein the annealing step is conducted at a temperature greater than 650 °C and for a time period greater than 200 seconds and less than 800 seconds.

21. The method of claim 1 wherein said metal catalyst is chosen from the group consisting of aluminum, indium tin oxide, nickel, cobalt, palladium and germanium.

22. A method of fabricating a polysilicon film, comprising the steps of:

providing a substrate;

depositing an amorphous silicon film on the substrate by the process of physical vapor deposition;

after deposition of said amorphous silicon film, depositing a metal catalyst film on selected regions of the amorphous silicon film; and

annealing the amorphous silicon film and the metal catalyst film to form a crystallized silicon film by pure metal induced crystallization in said selected regions.